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10/762,864	01/21/2004	Wilson Wong	174/295	5928

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EXAMINER	
FOTAKIS, ARISTOCRATIS	

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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,864	WONG ET AL.	
	Examiner	Art Unit	
	ARISTOCRATIS FOTAKIS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/19/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3 - 8, 10 - 12, 14 - 16, 20 - 22, 24, 26 - 28, 30, 32 - 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12, 14 – 16, 28, 35 and 43* is/are allowed.

6)☒ Claim(s) *1, 3 - 8, 10 - 11, 21 - 22, 24, 26 - 27, 30, 32 - 34, 36 - 39, 41 - 42* is/are rejected.

7)☒ Claim(s) *20, 40 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 22 is objected to because of the following informalities: The claim recites of "wherein the processing circuitry operates" in lines 5 – 6 and should be corrected to "wherein the **first** processing circuitry operates". Appropriate correction is required.

Claim 30 is objected to because of the following informalities: The claim recites of "first control signal**s**" in line 7 and should be corrected to "first control signal". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 20 - 22 and 40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 22 was amended to recite of

"a training pattern circuitry that computes a second training pattern". According to the specification, "*a predetermined training pattern is stored in element 176*" (Paragraph 0033) (training pattern circuitry). Therefore the disclosure does not support the amended limitation of computing the training pattern.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20 – 22, 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites of a "first processing circuitry for computing **an error signal**". Claim 21 recites of "wherein the first processing circuitry performs an algorithm to compute **the second error signal**". Claim 40 recites of "wherein the first processing circuitry…..computes **a first error signal**" in lines 6 – 9. It is not clear if the first processing circuitry computes a plurality of error signals (*first and second error signals*) or if it computes a single error signal (*first and second error signals are the same and are the error signal*)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3 – 7, 26, 33, 38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki (US 20040071205) in view of WinSLAC Software User's Guide (1999).

Re claims 1, 26, 33, 38 and 41, Gorecki teaches of a circuitry (transceiver, Fig.4) for adaptively equalizing a data signal, the circuitry (Abstract) comprising: equalization implementation circuitry that includes a selectable number of taps, wherein the equalization implementation circuitry operates on the data signal (Paragraph 0042, 0043); programmable circuitry that is programmed by configuration data with a first value corresponding to a first number of taps (*user*, Paragraph 0046); processing circuitry that computes a second value corresponding to a second number of taps (*adaptive algorithm*, Paragraph 0044 – 0045); the user or system may select between the first and second numbers as the selectable number of taps selecting one of the first and second values only once (*initialization or start-up,* Paragraph 0112). However, Gorecki does not specifically teach of the selection circuitry in a receiver circuitry based on a control signal selecting one of the first and second values.

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software (Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry selecting either the output of the programmable circuitry or the processing circuitry controlled by the user in order to provide a more flexible and user-defined system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the equalization circuitry on the receiver so as to be able to monitor or compensate fast varying channel conditions.

Re claim 3, Gorecki teaches of the processing circuitry performing an algorithm to compute the second number (Paragraph 0045).

Re claim 4, Gorecki teaches of a memory coupled to the processor programmable logic device circuitry coupled to the processor circuitry and the memory (Paragraph 0112).

Re claims 5 - 6, Gorecki teaches of a printed circuit board comprising: a memory mounted on the printed circuit board and coupled to the programmable logic device circuitry (Paragraph 0112).

Re claim 7, Gorecki teaches of the printed circuit board further comprising: processor circuitry mounted on the printed circuit board and coupled to the programmable logic device circuitry (Paragraph 0112).

Claims 21 – 22, 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaynes et al (US US 2005/0047779) in view of WinSLAC Software User's Guide (1999).

Re claims 22, 30 and 36, Jaynes teaches of a receiver circuitry ([0011]) for adaptively equalizing a data signal (Paragraph 0008, Figure) comprising: a first processing circuitry for computing an error signal using a selectable training pattern (#70, #72, Figure), wherein the first processing circuitry operates on the received data signal (Figure); programmable circuitry that is programmed by configuration data with a first training pattern and outputs the first training pattern (operator, Figure); training pattern circuitry that outputs a second training pattern (external process, Figure); and a first selection circuitry that receives the first training pattern and second training pattern; selects one of the first and second training patterns (external process or operator, Figure, Paragraph 0023) at the time the programmable circuitry is being programmed by configuration data (*user,* Paragraphs 0046, 0050, 0112), wherein the selection circuitry selects one of the first and second training patterns only once while the processing circuitry operates the data signal (Paragraphs 0008, 0022 – 0023, 0026) and outputs the selected one of the first and second training patterns to the first processing circuitry..

However, Jaynes does not specifically teach of the selection circuitry receiving the first training pattern and second training pattern in parallel and selecting one of the training patterns based on a control signal from the programmable circuitry.

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software (Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry controlled by the user to select between a processed value and a programmers value in order to provide a more flexible and user-defined system.

Re claim 21, Jaynes teaches of the first processing circuitry performing an algorithm to compute the error signal using a training pattern (*the error generator is a processor*, Paragraph 0015).

Claims 8 – 11, 24, 27, 32, 34, 37, 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki in view of Lu (US 6,275,836) and further in view of WinSLAC Software User's Guide (1999).

Re claims 8, 10, 27, 34, 39 and 42, Gorecki teaches of a circuitry (transceiver, Fig.4) for adaptively equalizing a data signal comprising: equalization implementation circuitry for adjusting or controlling the spacing of the taps (Paragraph 0043), wherein the equalization implementation circuitry operates on the data signal; programmable

circuitry for adjusting or controlling the spacing of the taps programmed by configuration data (*user,* Paragraphs 0046, 0050, 0112); processing circuitry for adjusting or controlling the spacing of the taps (Paragraph 0044 – 0045); the programmable circuitry or the processing circuitry may generate one of the tap spacing (Paragraph 0112) only once (*initialization or start-up,* Paragraph 0112), while the equalization implementation circuitry operates on the data signal (Paragraph 0112 – 0116). However, Gorecki does not teach of a programmable circuitry and processing circuitry for allowing a first selection between integer spacing and fractional spacing to be specified as well as the selection circuitry selecting either the output of the programmable circuitry or the processing circuitry but the equalization effects performed by either one of the two circuitries. However, Gorecki does not specifically teach of the selection circuitry in a receiver circuitry based on a control signal selecting one of the first and second values.

Lu teaches of a programmable logic device circuitry for adaptively equalizing a received data signal (Abstract, Fig.3) comprising: equalization implementation circuitry including taps (interpolation filter) having a selected one of integer spacing and fractional spacing relative to the symbol rate of the data signal (Abstract, Lines 1 – 13, Fig.3); processing circuitry (#74, Fig.3) for computing a (second) selection (#76a, #76b, Fig.3) between integer spacing and fractional spacing (Abstract, Lines 9 – 13, Fig.3 and Col 7, Lines 17 – 29).

WinSLAC Software User's Guide discloses of equalization for both receive and transmit paths (page 4-15) controlled by user interface dialogs in the WinSLAC software

(Page 3-5). The Guide further discloses of a selection circuitry based on a control signal (user interface) selecting one of a first value (*Calc or calculate*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19) and a second value (*Set*, 4.6 SLAC Menu, Pages 4 – 17 to 4 - 19).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided the option to the user to choose between a fixed or fractional spacing depending on the incoming sampling rate for a good equalizer performance. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the selection circuitry selecting either the output of the programmable circuitry or the processing circuitry controlled by the user in order to provide a more flexible and user-defined system. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the equalization circuitry on the receiver so as to be able to monitor or compensate fast varying channel conditions.

Re claim 11, Gorecki, Lu and WinSLAC Software User's Guide teach of all the limitations of claim 8. Lu teaches of the fractional spacing is a selectable fraction of the symbol period (1/fs, sampling rate f_s, Col 7, Lines 48 – 62), wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction (see claim rejection above).

Re claims 24, 32 and 37, Gorecki, Lu and WinSLAC Software User's Guide teach of a receiver circuitry for adaptively equalizing a data signal as discussed above in claims 8 – 11, comprising: equalization implementation circuitry, in the receiver circuitry, having at least one sampling point with a selectable location relative to a bit period of the received signal (*The symbol period of the tap spacing's is the inverse of the sampling frequency. Changing the tap spacing (as taught by Gorecki) will change the location of the sampling points*), wherein the equalization implementation circuitry operates on the data signal; programmable circuitry that is programmed by configuration data with a first value corresponding to a first location of the sampling point and outputs the first value and a control signal; processing circuitry that computes a second value corresponding to a second location of the sampling point and outputs the second value in parallel with the first value; and selection circuitry that: receives the control signal from the programmable circuitry, the first value and the second value in parallel (*receiving two values in parallel and selecting only one as disclosed by WinSLAC Software User's Guide*); selects, based on the control signal, one of the first and second values at the time the programmable circuitry is being programmed by the configuration data, wherein the selection circuitry selects one of the first and second values only once, while the equalization implementation circuitry operates on the data signal; and outputs the selected one of the first and second values to the equalization implementation circuitry, wherein the location of the at least one sampling point of the equalization implementation circuitry corresponds to the selected one of the first and second values.

Allowable Subject Matter

Claims 12, 14 – 16, 28, 35 and 43 are allowed.

Claims 20, 40 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed December 19, 2008 have been fully considered but they are not persuasive.

Applicants submit that Lu discusses the selection of fractional or integer sampling rates of an interpolation filter and does not show or suggest the selection between integer and fractional filter tap spacing.

Examiner submits that Gorecki teaches of computing or programming the tap spacing. The reference of Lu was brought to disclose the selection of fractional or integer spacing. Eventhough Lu may disclose fractional and integer sampling rates, the symbol period of the tap spacings is the inverse of the sampling rate.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aristocratis Fotakis/

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611